REMARKS

Claims 1-4 and 6-18 are all the claims pending in the application. Claim 5 has been incorporated into independent claim 1 and is therefore cancelled, above. Claims 1-4 and 16-18 stand rejected under 35 U.S.C. §102(b) as being anticipated by Chan et al. (US Patent No. 5,255,230), hereinafter referred to as "Chan". Applicants respectfully traverse this rejection based on the following discussion.

A. The Rejection Based on Chan

In rejecting independent claims 1, 8, and 14, the Office Action proposes that Chan anticipates the claimed invention by disclosing an apparatus that connects conductive lines of cells within an array together as if they were a single cell. However, as shown in greater detail below, Chan only discloses some additional transistors that are utilized to disconnect the memory cells from the bitlines and to connect all bitlines together. Chan does not teach or suggest the claimed invention which connects all significant conductive lines together to allow the entire array to be tested as a single cell.

More specifically, the invention wires together all cells within the array to allow the cells to be testable as if they were a single cell. More specifically, within the array, all bit lines, word lines, N-wells, interior grounds, and interior voltages are wired in common to enable the array to be characterized for different components of leakage. As shown in Applicants' Figure 1, the N-wells 105-108 are connected to a common N-well line 127 by connecting lines 125, 126. Similarly, bit line complement lines 120, 121 are connected to a common bit line complement line 124 by connecting lines 122, 123. Also, the bit lines 115, 116 are connected to a common bit line 119 by connecting lines 117, 118. Further, word lines 110, 111 are connected to a common word line 112. Each of the cells 100-103 includes an interior ground component (GND) and an interior voltage component (VDD). The ground component is connected to a common interior ground line 132 by connecting lines 130, 131; and the interior voltage component is connected to a common interior voltage line 137 by connecting lines 135, 136. In addition, the invention includes a ground line 140 connected to the substrate.

These features are clearly defined by the independent claims. For example, independent claim 1 defines that the "array of cells comprises a plurality of memory cells, word lines, bit lines, voltage lines, and ground lines, and wherein said conductive lines: join all word lines within said array as a single word line; join all bit lines within said array as a single bitline; join all voltage lines within said array as a single voltage line; and join all ground lines together within said array as a single ground line." Similarly, independent claim 8 defines the "conductive lines comprising: a common word line; a common bit line; a common bit line complement line; a common N-well voltage line; a common interior ground line; a common interior voltage line; and a common ground line." Also, independent claim 14 defines " joining: all word lines within said array as a single word line; all bit lines within said array as a single bitline; all voltage lines within said array as a single voltage line; and all ground lines together within said array as a single ground line." Therefore, Applicants submit that the independent claims clearly define that the invention wires together all cells within the array to allow the cells to be testable as if they were a single cell.

To the contrary, Chan only discusses that the bit lines should be isolated from their respective cells and connected together. More specifically, Chan explains that short circuit conditions may exist because of leakage conditions between different conductive traces on the same or different layers of the chip on which the memory cells are positioned. Chang states that it has been found by experience that the greatest chance for short circuit conditions in a CMOS SRAM memory array exists between either the bit or the bit# lines and the metallic conductors adjacent thereto. Consequently, by eliminating shorts between either of these bit lines and these adjacent metal conductors, a significant portion of cell shorting problems may be eliminated (see column 3, lines 55-65 of Chan).

Chan proposes that in order to test for short circuit conditions within an array, the memory transistors of the cells 10 should be disconnected from the bit and bit# lines and the value of the current through the bit lines and the bit# lines adjoining the cells of the array to be read. Chan states that theoretically, no current should flow through the bit lines once the cells have been disconnected from the bit and bit# lines. Consequently, the presence of current indicates that the memory array is defective. Chan provides that by connecting all of the bit and bit# lines of a memory array together, the total of all leakage

current may be summed to produce a significant detectable current if leakage is occurring. Moreover, the testing may be extended to better isolate the portion of the circuitry having a defect. For example, Chan states that all of the bit lines may be tested together or all of the bit# lines may be tested together to determine whether a short circuit condition affects either one or the other. Thus, Chan allows both the bit lines and the bit# lines of individual columns to be tested together or individually (the seas see column 3, line 66-column for line 18 of Chan).

Therefore, Applicants respectfully submit that Chan is limited to a structure that tests bitlines and does not teach or suggest the claimed invention as defined by independent claims 1, 8, and 14 which wires together all cells within the array to allow the cells to be testable as if they were a single cell. Therefore, Applicants submit that independent claims 1, 8, and 14 are not anticipated and are patentable over Chan. Further, dependent claims 2-4, 6, 7, 9-13, and 15-18 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-4 and 6-18, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

10/064,302

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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